USB Type-C ENGINEERING CHANGE NOTICE

Title: Handling EPR exits
Applied to: USB Type-C Specification Release 2.3, Oct 2023

Brief description of the functional changes proposed:
When a source disconnects after sourcing 48V it must get VBUS below vSafe0V within tSafe0V, which is the same value for SPR and EPR. This can be accomplished with a switch that disconnects the power supply from VBUS, leaving a smaller capacitance to discharge. However, if the device is quickly reconnected the power supply may still not have discharged down to 5V before the system is required to provide VBUS (tVBUSOn). There is an analogous scenario defined in USB PD after a hard reset, and the tSrcRecover parameter is given a longer time for EPR.

Benefits as a result of the proposed changes:
Allow an EPR source adequate time to discharge its power supply before applying 5V.

An assessment of the impact to the existing revision and systems that currently conform to the USB specification:
Should have no impact as it is a relaxation. Sinks wait indefinitely until VBUS is turned on in the state-machine.

An analysis of the hardware implications:
Reduces hardware complexity.

An analysis of the software implications:
May require updates to take advantage of the relaxation.

An analysis of the compliance testing implications:
No impact

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Actual Change Requested

(a). 4.5.2.2.8.2 Exiting from AttachWait.SRC State

From Text:

The port ***shall*** transition to ***Attached.SRC*** when VBUS is at ***vSafe0V*** and the ***SRC.Rd*** state is detected on exactly one of the CC1 or CC2 pins for at least ***tCCDebounce***.

To Text:

The port ***shall*** transition to ***Attached.SRC*** when VBUS is at ***vSafe0V*** and the ***SRC.Rd*** state is detected on exactly one of the CC1 or CC2 pins for at least ***tCCDebounce*** and V_{BULK} is ready to supply VBUS at vSafe5V. The port ***shall*** have V_{BULK} ready to supply VBUS within ***tBulkDisch*** of exiting previous ***Attached.SRC***.

(b). Table 4-32 VBUS and VCONN Timing Parameters

New Text:

tBulkDisch	0 ms	275 ms	From exit of Attached.SRC with VBUS ≤21V until the source is prepared to enable VBUS.
		700 ms	From exit of Attached.SRC with VBUS >21V until the source is prepared to enable VBUS.

(c). Section 4.11.2 Below Table 4-32

New Figure/Text:

Figure 1 shows an example source in order to illustrate the tBulkDisch parameter in conjunction with Figure 2 and Figure 3.

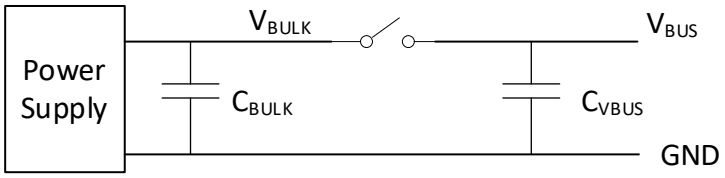

Figure 1 Source implementation example.

Figure 2 shows a scenario following a contract with V_{BUS} above 21V. In this example system, the tCCDebounce timer completes before the source is ready to supply V_{BUS} at vSafe5V since V_{BULK} > vSafe5V. Note that many implementations will discharge V_{BUS} below vSafe0V much faster than tVbusOFF (max).

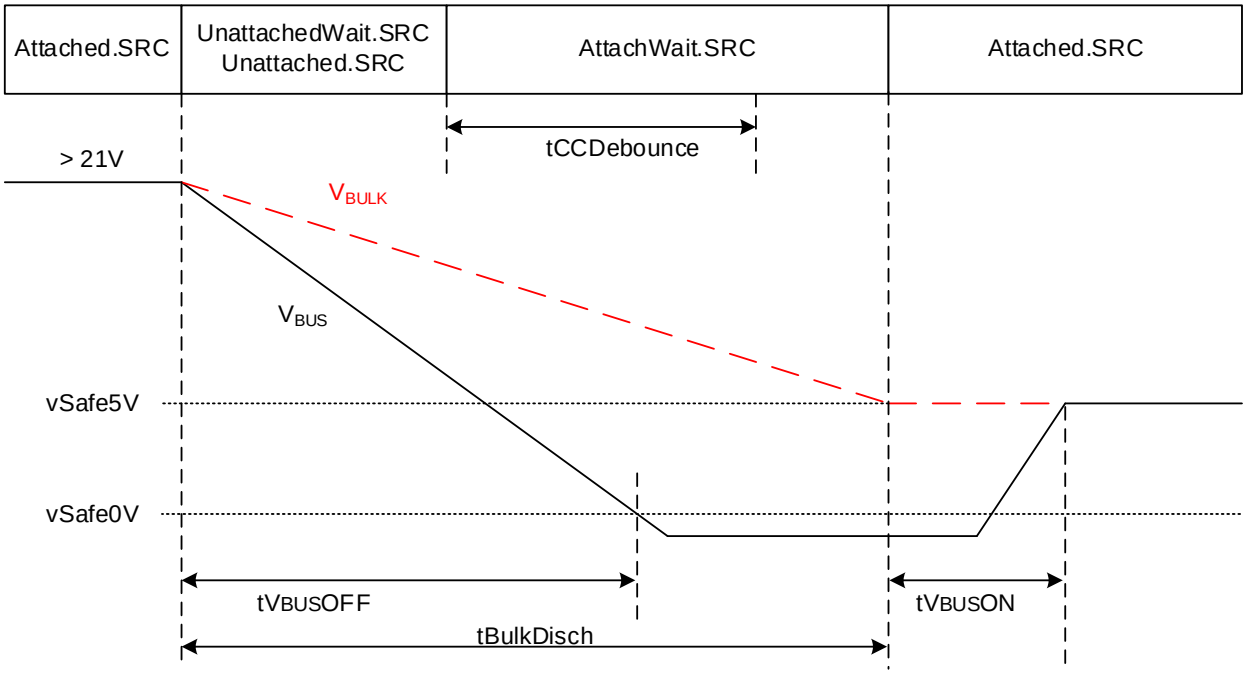

Figure 2 Exiting from Attached.SRC with slow discharging V_{BULK}.

Figure 3 shows a scenario following a contract with VBUS at 21V or below. In this example system, the V_{BULK} is discharged to vSafe5V before the tCCDebounce timer completes. Note that many implementations will discharge VBUS below vSafe0V much faster than tVbusOFF (max).

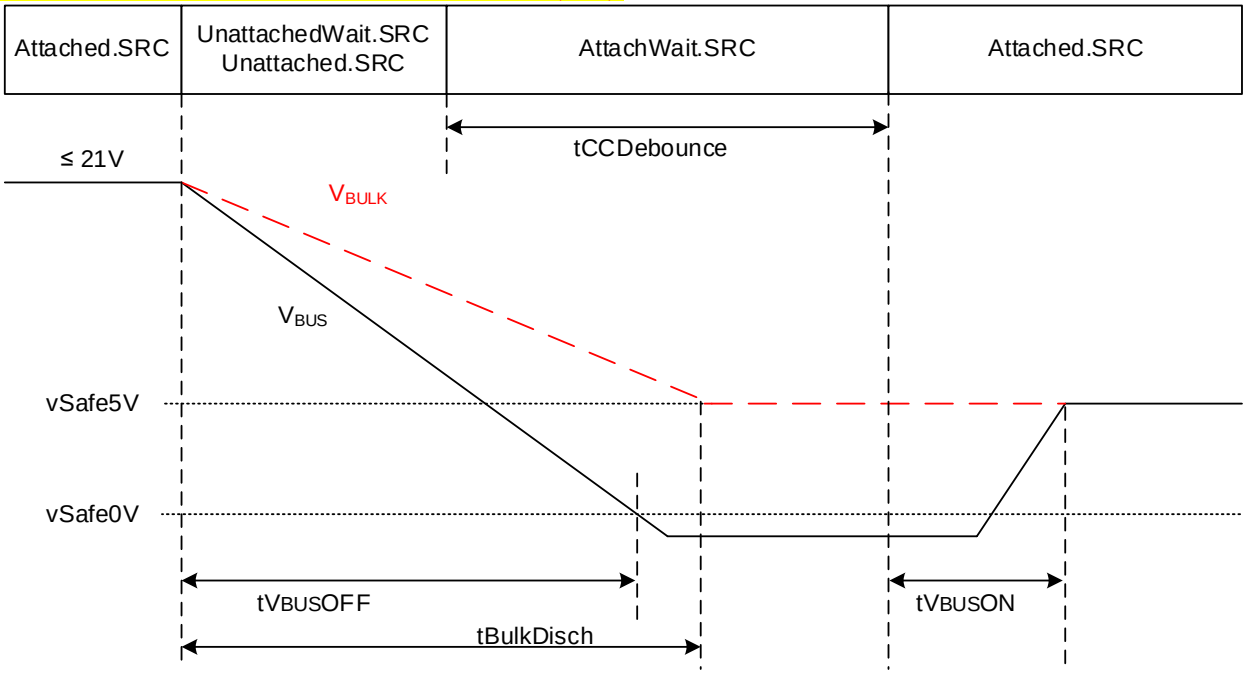

Figure 3 Exiting from Attached.SRC with fast discharging V_{BULK}.